This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,768	04/19/2001	Haw-Jyh Liaw	60809-0080-us	2900

38426 7590 06/23/2004

PENNIE & EDMONDS LLP/ RAMBUS INC.
3300 HILLVIEW AVENUE
PALO ALTO, CA 94304

EXAMINER
MYERS, PAUL R

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 06/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/839,768	LIAW ET AL.
	Examiner	Art Unit
	Paul R. Myers	2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/17/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 14, 29, 38 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Cooke et al PN 3,659,205.

3. Claims 14, 29, 38 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by OI JP 59-4204.

4. Claims 14, 29, 38 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Yamada et al PN 5,018,000.

5. Claims 14-15, 17, 20-21, 29, 31, 33, 38-40 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Buck et al PN 4,310,809.

In regards to claims 14, 29, 38: Buck et al teaches an apparatus comprising: a first substrate (Figure 2); a first signal trace (54) disposed on a surface of the first substrate, a connector (35) coupled to the first signal trace (54); and a first capacitor (62) including: a first capacitor electrode connected to a junction point between the connector and the first signal trace (35); and a second capacitor electrode coupled to a node that is at a supply potential (GND).

In regards to claims 15, 31, 39: Buck et al teaches one of the first and second capacitor electrodes comprises a conductive pad disposed on the surface of the first substrate (39).

In regards to claims 17, 33: Buck et al teaches the supply potential being a ground.

In regards to claim 20: Buck et al teaches the signal trace being a microstrip.

In regards to claim 21: Buck et al teaches the substrate is a printed circuit board.

In regards to claim 40: Buck et al teaches varied width of the conductor segments.

6. Claims 14, 17, 20-21, 25, 29, 33, 38 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Schwent et al PN 5,363,071.

In regards to claims 14, 29, 38: Schwent et al teaches an apparatus comprising: a first substrate (802); a first signal trace (502) disposed on a surface of the first substrate (802), a connector (413) coupled to the first signal trace (502); and a first capacitor (706) including: a first capacitor electrode connected to a junction point between the connector and the first signal trace (708); and a second capacitor electrode coupled to a node that is at a supply potential (GND).

In regards to claims 17, 33: Schwent et al teaches the supply potential being a ground.

In regards to claim 20: Schwent et al teaches the signal trace being a microstrip.

In regards to claim 21: Schwent et al teaches the substrate is a printed circuit board.

In regards to claim 25: Schwent et al teaches a second substrate; a second signal trace disposed on a surface of the second substrate; a connector interface coupled to the second signal trace, to mate with the connector and electrically couple the second signal trace to the first signal trace; a second capacitor including: a first capacitor electrode connected at a junction point between the connector interface and the second signal trace; and a second capacitor electrode coupled to a node that is at the supply potential.

7. Claims 14, 17, 20-21, 23-24, 27, 29, 33, 35-38, 43 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Maruhashi PN 5,363,071.

In regards to claims 14, 29, 38: Maruhashi teaches an apparatus comprising: a first substrate (Column 1 lines 43-56); a first signal trace (1) disposed on a surface of the first substrate, a connector (4) coupled to the first signal trace (1 at 6); and a first capacitor (2) including: a first capacitor electrode connected to a junction point between the connector and the first signal trace (6); and a second capacitor electrode coupled to a node that is at a supply potential (3).

In regards to claims 17, 33: Maruhashi teaches the supply potential being a ground.

In regards to claim 20: Maruhashi teaches the signal trace being a microstrip.

In regards to claim 21: Maruhashi teaches the substrate is a printed circuit board.

In regards to claims 23, 36: Maruhashi teaches the connector includes a first impedance value, and the first signal trace includes a second impedance value, the first impedance value being different from the second impedance value.

In regards to claims 24, 37: Maruhashi teaches the capacitor reduces the difference between the first and second impedance values.

In regards to claims 35, 43: Maruhashi teaches a dielectric.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 16, 18-19, 22, 35, 42-43 rejected under 35 U.S.C. 103(a) as being unpatentable over Maruhashi PN 5,384,558 in view of Wark et al PN 5,982,018.

In regards to claim 16: Maruhashi teaches high frequency coupling including a capacitor to ground. Maruhashi does not teach the device including memory modules. Wark et al teaches memory modules including capacitors coupled to ground. Wark et al does not expressly teach the location of the capacitor coupling being at a junction point between the connectors and the signal traces. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use memory modules as the circuits in Maruhashi because this would have allowed for increased speed of memory accessing.

In regards to claims 18, 42: Wark teaches a ground plate beneath the first substrate.

In regards to claims 19, 35, 43: Wark teaches a dielectric between the plates.

In regards to claim 22: Wark teaches a pin.

10. Claims 25-28, 30, 32, 44-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maruhashi PN 5,384,558 in view of Ammon PN 3,868,162.

In regards to claims 25-26: Maruhashi teaches the substrate, connector and capacitor to ground described above. Maruhashi only teaches one board. Ammon teaches a motherboard and a daughter board. It would have been obvious to a person of ordinary skill in the art at the time of the invention to apply Maruhashi system to both the motherboard and daughter board of Ammon because this would have allowed for proper impedance matching including radio frequency.

In regards to claim 27: Maruhashi teaches the capacitor reduces the difference between the first and second impedance values.

In regards to claims 28, 30, 44: Ammon teaches conductive pads at the edge of the substrates.

In regards to claims 32, 45: Ammon teaches a socket.

11. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maruhashi PN 5,384,558 in view of Geiszler PN 3,359,510.

In regards to claim 41: Maruhashi teaches handling impedance matching. Maruhashi does not teach varying the width of the conductor for impedance matching. Geiszler teaches varying the width of a conductor for impedance matching. It would have been obvious to a person of ordinary skill in the art to use width varying for impedance matching because this would have allowed for handling microwave frequency.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 703 305 9656. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703 305 4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PRM
June 18, 2004

PAUL R. MYERS
PRIMARY EXAMINER